COMPUTING OPTIMIZATION WITH REAL NUMBERS THROUGH ARITHMETIC UNITS

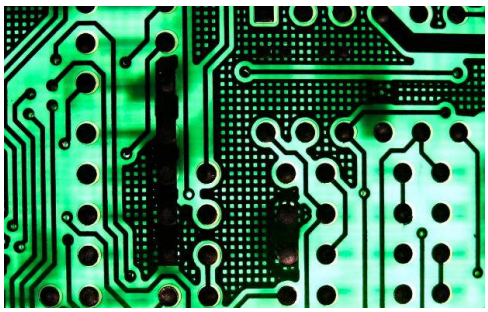
Description:

The present invention allows the implementation of more efficient digital information processing systems (faster, smaller area, lower cost, lower energy consumption). This is achieved through the use of a modification of the real number encoding formats, applicable to the vast majority of current formats, which simplifies the circuits that process said formats. Specifically, they allow the rounding and change of sign to be carried out at little cost. This simplification at a logical level produces the simultaneous optimization of area, speed and consumption of the arithmetic units that process said numbers, without negatively affecting the rest of the elements of the digital system.

Keywords:
Arithmetic Units, Digital Circuits, Fixed Point, Floating Point

Sectors:
ICT, Electronics, Engineering

Areas:
Telecommunications, Hardware / Devices / Components, Technological Improvements



Advantages:

Simultaneous reduction of area, consumption and delay of the processing circuits. Valid for any digital system based on real number computation, including fixed point and floating point circuits. Valid for any implementation technology, including FPGA or ASIC. Valid both for basic operations (addition, multiplication, ...) and for more complex ones (square root, trigonometric, ...)

Uses and Applications:

Implementation of digital systems based on numerical computing, for example: digital signal processing (DSPs), communications, audio, video, graphic processing, simulation of physical systems, industrial control, home automation, automotive, neural networks, robotics, etc. Implementation of arithmetic units in processors.

Patent Number: WO2015144950
Applicants: Universidad De Málaga
Inventors: Francisco Javier Hormigo Aguilar, Julio Villalba Moreno
Filing Date: 28/03/2014
Protection Level: National (Spain) and international
Processing Status: Spanish patent